In the claims:

Please amend claims 1, 5, 12, and 16, and cancel claims 2-4 and 13-15.

For the Examiner's convenience, all claims ***pending*** *are indicated below.*

1. (Amended Three Times) A display controller for receiving video data from a data bus in a component YUV format and storing the video data to a display memory in a pixel video format, said display controller comprising:

a bus interface [means], coupled to the data bus, for receiving video data in a component YUV format and corresponding video data addresses within a predetermined address range; [and]

a display memory controller, coupled to said bus interface [means], for receiving video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range and for storing said video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory[.]:

wherein said video data comprises luminance and chrominance difference data and said component YUV format

comprises a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data; and

D' concl.

wherein said display memory controller stores the first contiguous block of luminance data in at least one byte lane within the display memory and stores the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory.

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2. (Canceled) The display controller of claim 1 wherein said video data comprises luminance and chrominance difference data and said component YUV format comprises a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data.

3. (Canceled) The display controller of claim 2 wherein said display memory controller receives the first contiguous block of luminance data and stores the first contiguous block of luminance data in at least one byte lane within the display memory.

4. (Canceled) The display controller of claim 3 wherein said display memory controller receives the at least a second contiguous block of chrominance difference data and stores the

at least a second contiguous block of chrominance difference data in at least another byte ~~lane~~ within the display memory.

D2 5. (Amended) The display controller of claim [4] 1, wherein said first contiguous block of luminance data comprises one frame of luminance data.

6. (Unchanged) The display controller of claim 5, wherein said at least a second contiguous block of chrominance difference data comprises one frame of chrominance difference data.

7. (Unchanged) The display controller of claim 6 wherein said at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of luminance data for one line of one frame of video data.

8. (Unchanged) The display controller of claim 7 wherein said at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of chrominance difference data for one line of one frame of video data.

9. (Unchanged) The display controller of claim 8, wherein said chrominance difference data is stored in every other line of each of said plurality of pairs of byte lanes and said display controller further comprises a bit block transfer engine for transferring blocks of data within the display memory, wherein said bit block transfer engine replicates chrominance data from every other line of said plurality of pairs of byte lanes to a corresponding adjacent line within said plurality of pairs of byte lanes.

10. (Unchanged) The display controller of claim 9 wherein said bit block transfer engine replicates chrominance data after said display memory controller has completed storing one frame of video data in the display memory.

11. (Unchanged) The display controller of claim 10 wherein said display controller outputs a signal through said bus interface to a host processor indicating completion of a bit block transfer operation.

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12. (Amended Three Times) A method for assisting decoding of video data partially decoded in a host processor, said method comprising the steps of:

receiving, in a display controller, video data in a component YUV format in contiguous successive streams of luminance and chrominance difference data and corresponding video data addresses within a predetermined address range, [and]

storing the video data by directing separate luminance and chrominance difference data into predetermined memory portions according to a predetermined memory aperture mapped to a display memory so as to store said video data in a pixel video format in the display memory[.],

D3 cont.

wherein said video data comprises luminance and chrominance difference data and said component YUV format comprises a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data, and

storing, by use of a display memory controller, the first contiguous block of luminance data in at least one byte lane within the display memory and the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory.

13. (Canceled) The method of claim 12 wherein the video data comprises luminance and chrominance difference data and the component YUV format comprises a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data.

14. (Canceled) The method of claim 13 wherein the step of storing comprises the step of storing the first contiguous block of luminance data in at least one byte lane within the display memory.

15. (Canceled) The method of claim 14 wherein the step of storing further comprises the step of storing the at least a second contiguous block of chrominance difference data in a least another byte lane within the display memory.

16. (Amended) The method of claim [15] 12, wherein the first contiguous block of luminance data comprises one frame of luminance data.

17. (Unchanged) The method of claim 16, wherein the at least a second contiguous block of chrominance difference data comprises one frame of chrominance difference data.

18. (Unchanged) The method of claim 17 wherein the at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes

for storing pairs of luminance data for one line of one frame of video data.

19. (Unchanged) The method of claim 18 wherein the at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of chrominance difference data for one line of one frame of video data.

20. (Unchanged) The method of claim 19, wherein the step of storing further comprises the steps of:

storing chrominance difference data in every other line of each of the plurality of pairs of byte lanes, and

replicating, in a bit block transfer engine within the display controller, chrominance data from every other line of the plurality of pairs of byte lanes to a corresponding adjacent line within the plurality of pairs of byte lanes.

21. (Unchanged) The method of claim 20 wherein the bit block transfer engine replicates chrominance data after the display memory controller has completed storing one frame of video data in the display memory.

22. (Unchanged) The method of claim 21 further comprising the step of outputting a signal to a host processor indicating completion of a ~~bit~~ block transfer operation.

REMARKS

The undersigned thanks Examiner Nguyen for granting the telephone interviews regarding this application on June 24, 1999 and June 25, 1999.

Claims 1-22 are rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over by U.S. Patent No. 5,604,514 to Hancock ("Hancock '514") in view of U.S. Patent No. 5,699,277 to Munson et al. ("Munson '277"), further in view of U.S. Patent No. 5,666,137 to Coelho et al. ("Coelho '137"), and further in view of U.S. Patent 5,526,025 to Selwan et al. ("Selwan '025"). The Applicant respectfully traverses this rejection for the reasons presented below.

Independent claim 1 now recites a display controller that includes:

a bus interface , coupled to the data bus, for receiving video data in a component YUV format and